Qualification Results Summary, Automotive Grade 1 at ADLK Fab

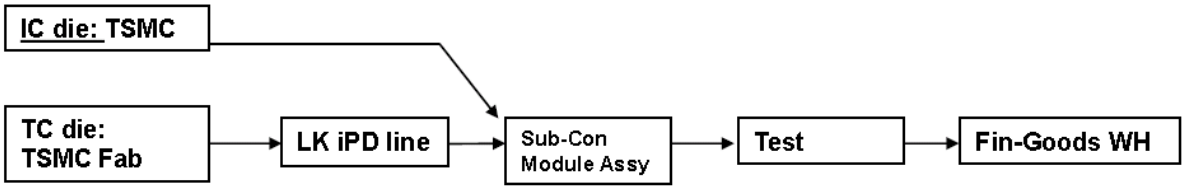
QUALIFICATION RESULTS			
TEST	**SPECIFICATION**	**SAMPLE SIZE**	**RESULTS**
Autoclave (AC)[1,2]	JEDEC *JESD22-A102*	**1*77**	**Pass**
Highly Accelerated Stress Test (HAST)[1,2]	JEDEC *JESD22-A110*	**1*77**	**Pass**
Temperature Cycle (TC)[1,2]	JEDEC *JESD22-A104*	**1*77**	**Pass**
Solder Heat Resistance (SHR)[1,2]	JEDEC/IPC *J-STD-020*	**1*30**	**Pass**
High Temperature Storage Life (HTSL)[2]	JEDEC *JESD22-A103*	**1*45**	**Pass**
High Temperature Operating Life (HTOL)[1,2]	JEDEC *JESD22-A108*	**1*77**	**Pass**
Early Life Failure (ELF)[2]	AEC *AEC-Q100-008*	**3*800**	**Pass**
Electrostatic Discharge[2] *Field-Induced Charged Device Model*	JEDEC *JESD22-C101*	**3/voltage**	**Pass 1250V**
Electrostatic Discharge[2] *Human Body Model*	ESDA/JEDEC *JS-001*	**3/voltage**	**Pass 3500V**
Electrostatic Discharge[2] *Machine Model*	JEDEC *JESD22-A115*	**3/voltage**	**Pass 100V**
Latch Up[2]	JEDEC *JESD78*	**3/current**	**Pass 200mA**

[1] These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 3 preconditioning consists of the following: 1. Bake – 24 hours at 125°C; 2. Soak – unbiased soak for 168 hours at 85°C, 85%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260°C. TC samples were subjected to wire-pull test after 500 cycles with results within specification limits.
[2] These samples were tested per AECQ-100.

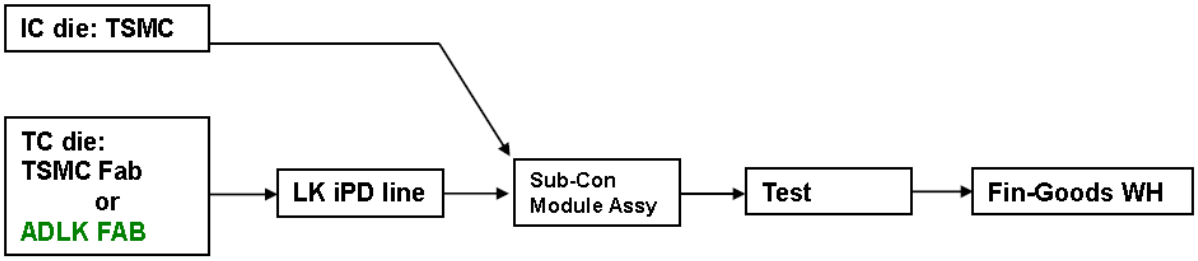
PCN 15_0032:

Alternate fab source for ISO TC start silicon die.
To enable additional wafer fabrication capacity.

Current Flow:



Alternate Flow:



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